unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets; and

wherein additional said requesters may be coupled to the internal switching fabric adding additional said requestor connection ports.

Claim 25 (new)

The claim of claim 24 further comprising one or more arbiters one that couple to said decoder/router elements and arbitrates said requests between said requestor connection ports and said target connection ports to said designated target.

Claim 26 (new)

The claim of claim 24 wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port.

Claim 27 (new)

The claim of claim 24 wherein said request routed to said designated target by said decoder/router element further comprises a registered, point-to-point signal that further comprises a plurality of pipeline stages.

Amendments to the Drawings

The attached sheet of drawings includes the requested changes to FIG. 1. This sheet replaces the original sheet that includes FIG. 1.